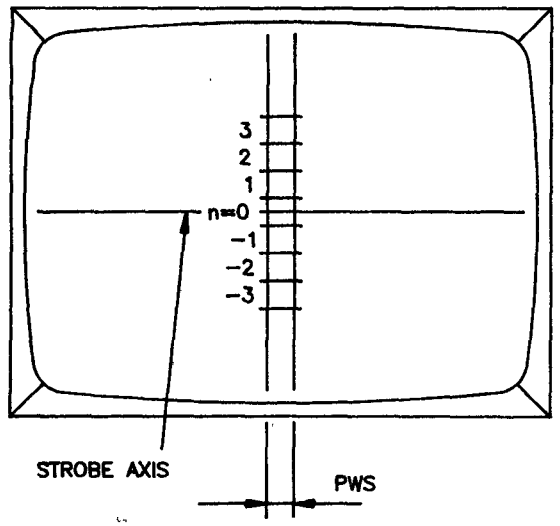

Fig. 2. Diagrammatic representation of a stack of pixels on a cro screen.

will paint the nth pixel in a given PWS is

$$P(n) = \Delta \cdot \rho(n\Delta) \approx (2/5N)\exp-(n^2/2N^2) \quad (2)$$

and the average number of paints/s will be

$$M(n) = f_s \cdot P(n) = (2f_s/5N)\exp-(n^2/2N^2). \quad (3)$$

The human eye has an integration time of about 0.06 s [6]. Even allowing for average phosphor persistence, light pulses emitted by a pixel will have a duration much less than this. Hence from each pixel the eye will be presented essentially with pulses of light in a pulse train where there is a pulse once each $\tau_s = (1/f_s)$ s with probability $P(n)$. It is this train which is integrated by the visual system to produce the sensory response. For a pixel to appear not to flicker requires reception on average of several pulses per integration time. A minimum of about 60/s would be typical. For the experiment to work at all this must be the case at least for the zeroth-level pixel ($n = 0$). We thus require

$$2f_s/5N = M_0 \quad (4)$$

where $M_0 \approx 60/s$ or more.

The eye will perceive the edge of the noise trace as being at a level where the picture starts flickering strongly. Typically this will occur when the average interval between pulses becomes comparable to the integration time, say around $M_e \approx 20/s$. The order of the pixel at which this occurs is then easily shown to be

$$n_e = N\sqrt{2\ln(M_0/M_e)} \quad (5)$$

and the edge appears at a displacement from the axis of the illuminated strip of

$$y_e = n_e\Delta = \sigma\sqrt{2\ln(M_0/M_e)}. \quad (6)$$

Let the system be pulsed with a square waveform (unity mark/space ratio) which is adjusted in amplitude until a TSNR is obtained. Then the trace displacement at the top of the square wave will be $y_s = 2y_e$ and the corresponding signal to noise ratio is

$$S/N|_{dB} = 9.6 + 10\log_{10}\{\log_{10}(M_0/M_e)\}. \quad (7)$$

This result is not sensitive to the precise choice of M_0/M_e and a wide range of observers exercising no great care in setting up the experiment can be expected to obtain similar results. Selection of $3 < M_0/M_e < 6$ produces only about a ± 1 dB variation about a mean of 7.5 dB. Experimental evidence has led to a consensus that TSNR corresponds to a signal to noise ratio of 8 dB. This agrees, perhaps surprisingly well, with the outcome of the somewhat ad hoc theory developed in this paper. More to the point, though, is that the theory can explain why this rather ill-defined experiment yields fairly consistent results independently of observer or equipment.

III. Conclusion

A theory based on the physiology of the human eye has been presented which explains the observed consistency of TSNR as a simple means for measuring receiver sensitivity. The theory arrives at the finding that under a wide range of conditions TSNR corresponds to a signal to noise ratio of 7.5 ± 1 dB, a result which compares well with a generally accepted empirical value of 8 dB.

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Cryogenic Performance of a GaAs MMIC Distributed Amplifier

C. R. Moore, W. C. Trimble, M. L. Edwards, and T. R. Sanderson

Abstract—**A three-stage GaAs MMIC distributed amplifier chip, fabricated to our design, was specially packaged in a two-chip, six-stage amplifier for cryogenic operation from 1 to 10 GHz. When immersed in liquid nitrogen a fourfold reduction in amplifier noise was observed over the 4 GHz to 8 GHz frequency range. This is in agreement with the generally observed scaling with ambient temperature (in Kelvin) for discrete GaAs FET amplifiers.**

I. Introduction

GaAs MMIC technology shows great promise for enhancement of performance of broad-band (multioctave) devices. Integrating this technology with high-temperature superconductor devices will ideally require MMIC operation at cryogenic temperatures. In an effort to evaluate the possibilities and potential difficulties of operating GaAs MMIC devices at these temperatures, an internal research and development program was undertaken.

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The authors are with the Applied Physics Laboratory, Johns Hopkins University, Laurel, MD 20723.
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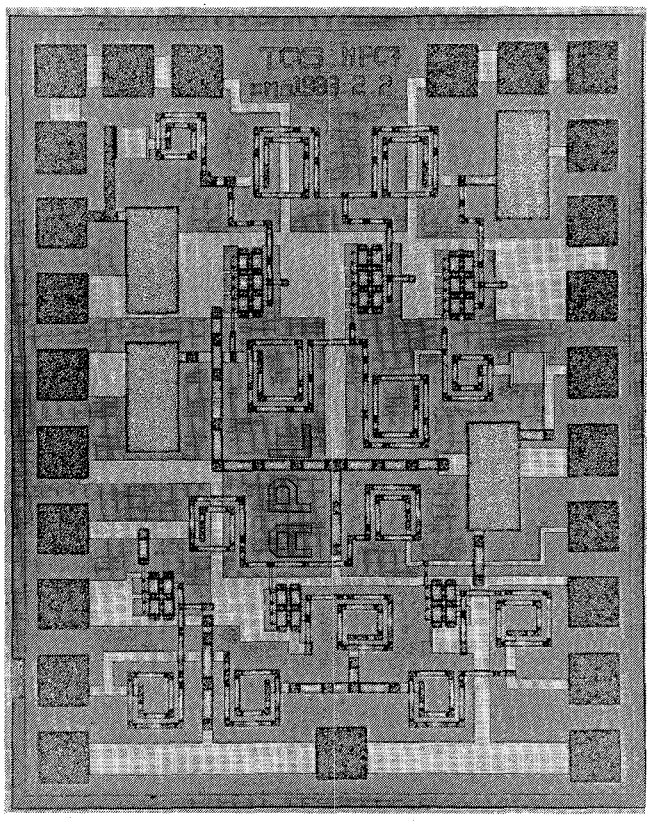

Fig. 1. Photomicrograph of the GaAs MMIC distributed amplifier. The 50 mil×62 mil (1280×1575 μm) chip contains two independent three-stage amplifiers of different design.

A lumped-element distributed amplifier topology was chosen for investigation in order to evaluate the adequacy of computer models, the effect of magnitude of various parasitic elements, and the resulting device performance over a wide frequency and temperature range. It was expected that cryogenic operation would result in an increase in gain and a reduction in noise figure, as is observed for discrete GaAs FET amplifiers [1]. Although room-temperature performance is not a good predictor for cryogenic performance [2], it is generally observed for well-behaved submicro-gate-length discrete GaAs devices that the amplifier noise temperature scales as the ratio of ambient temperature (in Kelvin) for operation down to at least 100 K ambient [3]. Our program was also directed toward devising ways to package multiple MMIC chips in such a way as to provide good thermal contact to a cold mounting surface, to permit repeated excursions from room temperature to cryogenic temperatures without mechanical failure, and to achieve acceptable microwave performance over a broad frequency range.

II. MMIC Design

The MMIC chip was fabricated by TriQuint Semiconductor, using their half micron analog (HA) process, under the Multi Project Chip program. The design analysis was facilitated by use of TouchStone and the layout was done using ICED, both running on a personal computer. A photomicrograph of the 50 mil×62 mil (1280×1575 μm) chip is shown in Fig. 1. Two independent distributed amplifiers are contained on each die.

The top half of the die contains an amplifier employing gate and drain line 50 Ω terminating resistors, bias decoupling capacitors, and input and output dc blocking capacitors. The three active devices are 0.5 μm gate length, six-finger×50 μm gate width MESFET's. This amplifier is termed a cascadable device, as it is a two-port amplifier matched to 50 Ω when a 300 pH bond wire inductance is included on the input and output of the packaged chip.

The lower half of the die contains a four-port distributed amplifier which is intended to be chained to another die to form an $N \times 3$ stage distributed amplifier. Again, the bond wires become part of the gate and drain lumped element transmission lines when the die is packaged. The three active devices are 0.5 μm gate length, four-finger×50 μm gate width MESFET's. An on-chip schematic diagram of this chainable amplifier is shown in Fig. 2.

Both amplifiers employ an LC network between each drain and its drain line connection for high-frequency peaking. The RF input and output bond pad connections are arranged so as to be bounded on either side by ground pads. This permits measurement of unpackaged die on a microwave wafer probe station. These measurements are useful in verifying the modeled performance and in de-embedding the package and test fixture. Both amplifiers were designed for operation from 0.25 GHz to 12.5 GHz, a $1\frac{1}{2}$ decade frequency range. Extensive room-temperature measurements and both linear and nonlinear modeling have been conducted on unpackaged and packaged chips. These confirm agreement between the models and measurements for gain, band-pass, and gain compression to typically less than 0.5 dB. The room-temperature noise parameters of one of our unpackaged cascadable chips were measured for us on a probe station by Eric Strid of Cascade Microtech. These results together with our simulated performance are shown in Fig. 3.

The element models used for design simulations were provided by TriQuint and EEsof and are for room-temperature operation only. The noise model in TouchStone utilized noise parameters provided by TriQuint as typical for the 0.5 μm MESFET in their HA process at room temperature. Our project resources did not permit any cryogenic measurements of individual MMIC components. Therefore no simulations of cryogenic performance were undertaken and no particular considerations could be made for cryogenic operation during the design phase.

III. Cryogenic Amplifier Package

For cryogenic tests it was desirable to include a significant number of MMIC elements in order to lend validity to any successful cryogenic performance. The chosen topology contains two chips chained together, thus forming a six-stage lumped-element distributed amplifier. The bond wires on the four RF ports of each chip become part of the gate and drain transmission lines of the two-chip amplifier. The resulting amplifier contains 26 MMIC lumped elements—six 200 μm MESFET's, six MIM capacitors, and 14 air bridge metal spiral inductors. Fifteen gold bond wires are employed to electrically connect the two chips to each other and to 50 Ω coplanar lines on the alumina MIC substrate. The substrate contains gate and drain terminating resistors, bias bypass capacitors, and input and output blocking capacitors. The amplifier was intended for cryogenic operation with a 1 to 10 GHz passband.

To accommodate temperature cycling to cryogenic temperatures, while minimizing the thermal gradient between the MMIC chips and the cold mounting block, a custom assembly process was developed. Although suitable for higher aspect ratio GaAs devices such as transistors the conventional gold tin eutectic chip mount process was not used because the high elastic modulus of this material could induce large stresses in the alumina substrate and GaAs MMIC chip. Also, because the thermal coefficient of expansion of gold tin eutectic is a nonlinear function of temperature, modeling the stresses induced by this material is not trivial. To avoid these potential problems a mounting process utilizing 80% In, 15% Pb, and 5% Ag solder (Indalloy #2) was developed. This solder was chosen because of

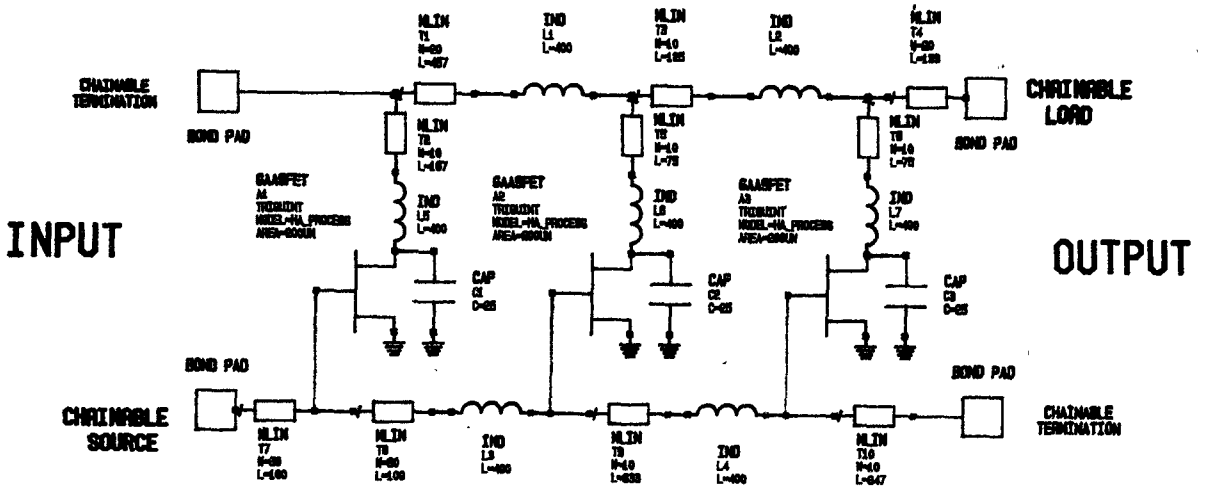

Fig. 2. Schematic diagram of the on-chip circuitry for the chainable distributed amplifier which was packaged in the two-chip cryogenic amplifier.

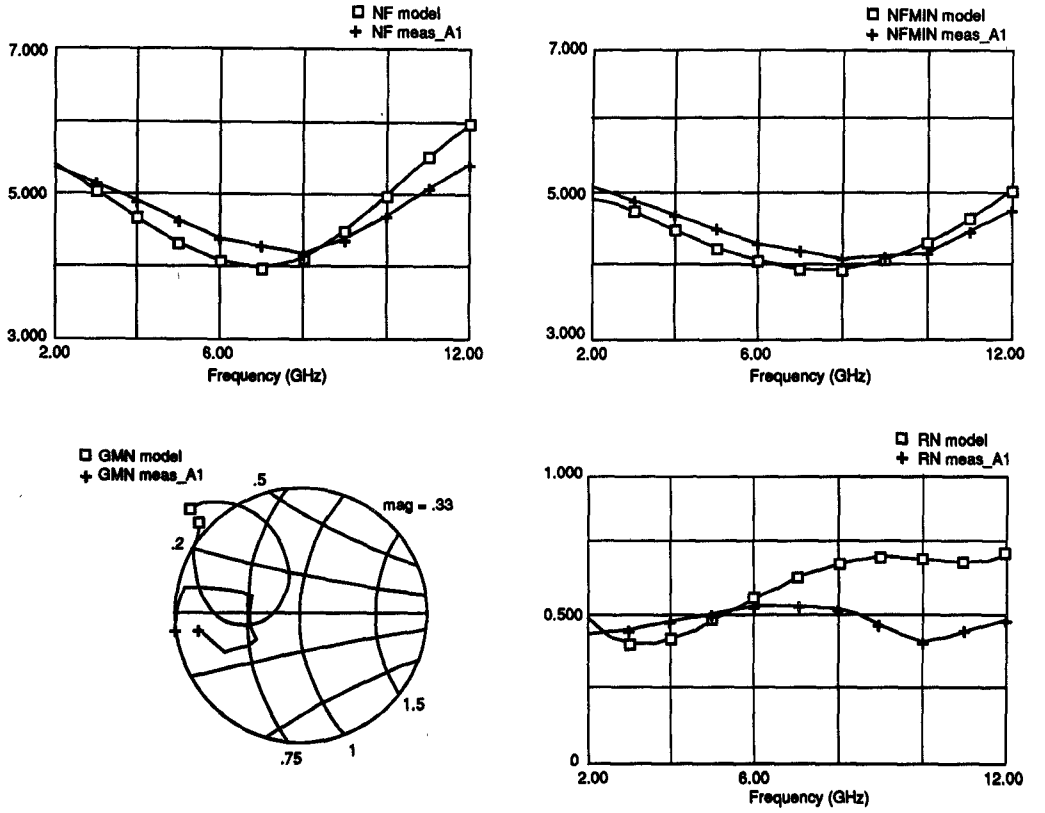

Fig. 3. Simulated and measured noise figure and noise parameters for the unpackaged cascadable distributed amplifier at room temperature. Bias conditions: $V_{ds} = 2.5$ V, $I_{ds} = 8$ mA ($\times 3$).

its low (160°C) reflow temperature and low elastic modulus and its plastic nature at low temperatures.

The first step in this custom process was to reflow solder the discrete components onto the chrome–copper–gold metallization on a 10 mil (0.25 mm) thick alumina substrate using Sn62 solder. This substrate was then reflow soldered to a 35 mil (0.88 mm) thick copper-clad molybdenum carrier using Indalloy #2 solder and RMA flux. This assembly was immediately solvent cleaned to remove all flux, argon plasma cleaned, and then placed back on a hot plate for attachment of the MMIC chips. An Indalloy #2 solder preform was placed in a window previously machined in the alumina substrate and the 7 mil (0.18 mm) thick MMIC chips were gently hand scrubbed to aid attachment to the copper clad molybdenum carrier with this preform. It is believed this fluxless reflow chip attachment process is made possible because of the cleaning action of the flux used during substrate reflow, the argon plasma preclean of the carrier, and a 10% HCl preclean of the solder preform.

Following fabrication of the circuit on the copper clad molybdenum carrier all wire-bonding was performed. The carrier was then bolted to an OFHC copper block which formed the bottom surface of the amplifier enclosure. Coaxial "K" connectors and dc filter feedthroughs were mounted to brass plates which bolted to the copper bottom block to form the sides of the

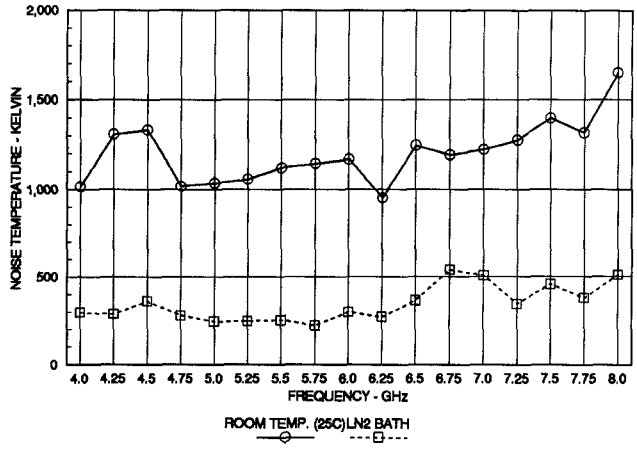

Fig. 4. Amplifier noise temperature of the two-chip, six-stage chained amplifier measured at room temperature and when immersed in liquid nitrogen. Bias conditions: $V_{ds} = 2.5$ V, $I_{ds} = 8$ mA ($\times 6$).

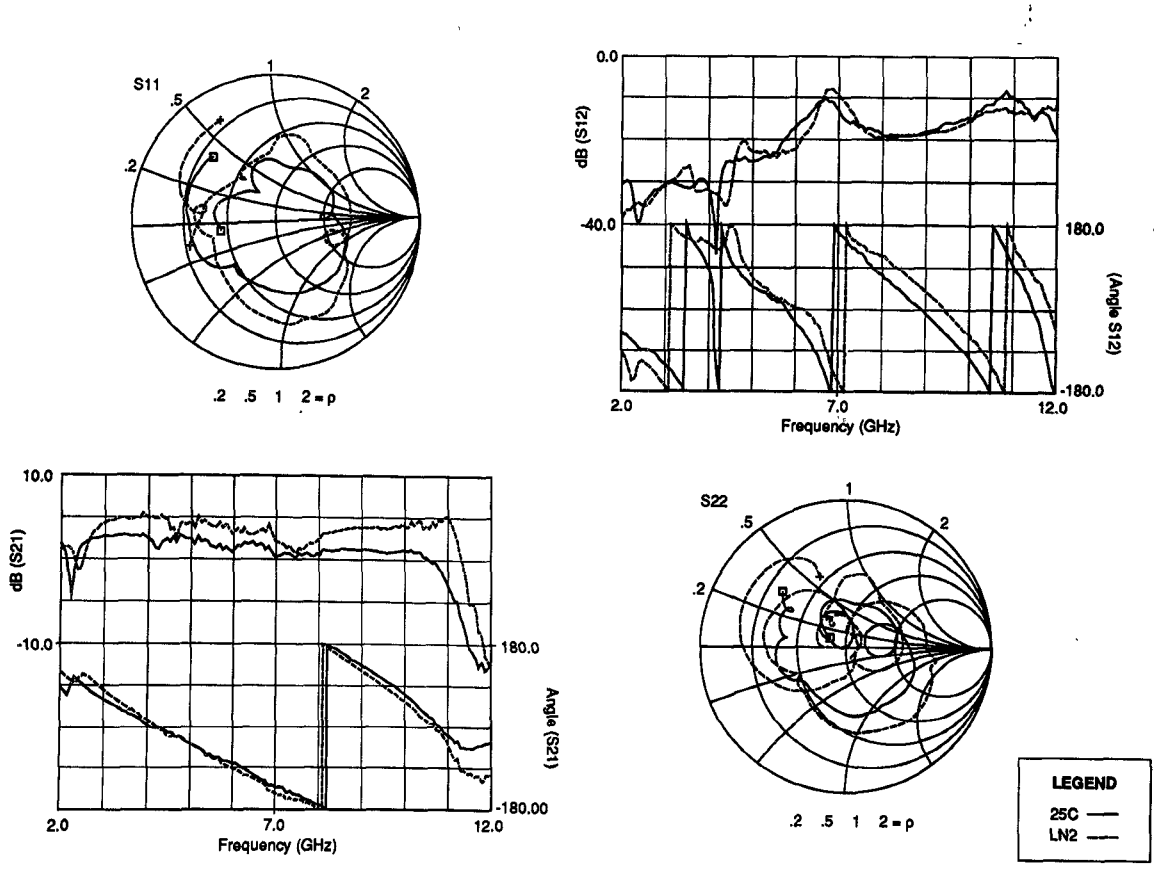

Fig. 5. S parameters of the two-chip, six-stage chained amplifier measured at room temperature and in a liquid nitrogen bath. Bias conditions: $V_{ds} = 2.5$ V, $I_{ds} = 8$ mA ($\times 6$).

enclosure. Conventional coplanar waveguide techniques were used to make interconnections between these components and the substrate metallization. A brass lid completed the amplifier enclosure.

IV. Test Configuration

The two-chip amplifier was characterized at room temperature and while immersed in liquid nitrogen (LN2) for gain and noise temperature with a Hewlett-Packard 8970S gain/noise measurement system. The RF input and output were thermally isolated with 8 in. (20 cm) lengths of 0.085-in.-diameter stainless steel semirigid coaxial cable. The amplifier was placed in the bottom of a polystyrene foam box and LN2 was added to just submerge the base of the amplifier unit up to the level of the RF connectors. The room-temperature measurements were repeated several hours later when the LN2 had boiled away and the amplifier had warmed to room temperature.

The amplifier was replaced with an SMA female/female adapter, which was also just barely submerged in LN2, for calibration of the test setup gain and noise contributions. Measurements were made in 250 MHz increments over the 4 to 8 GHz frequency range. These calibration data were used to assign on insertion loss and an effective physical temperature to

both the input and output coaxial lines at each frequency. These values were then used to remove the effect of the coaxial line from the measured amplifier data. The mean value of the effective coaxial line temperature when cooled in LN2 was 136 K and the standard deviation about the mean value over the frequency range was 36 K.

The accuracy of the noise temperature value calculated for the amplifier is dominated by the accuracy of the HP 8970S gain/noise measurement system. If this uncertainty is taken to be ± 0.25 dB, then the uncertainty in the amplifier noise is ± 30 K for the LN2 measurements and ± 80 K for the room-temperature measurements.

S parameters were measured with the two-chip amplifier at room and at LN2 temperature. These measurements utilized the previously described test setup in conjunction with a Wiltron 360 vector network analyzer. The room-temperature and cold (LN2) reflection, load, and transmission (through) calibrations were performed at the amplifier/stainless steel coax interface. The cold calibration was done with only the through adapter immersed in LN2 to avoid damaging the precision reflection and load elements. This has the effect of introducing an error in the phase reference plane owing to the uncalibrated change in the electrical length of the cold portion of the coaxial cable. The $S11$ and $S22$ magnitude is also in error because of the uncalibrated reduction in loss of the cold portion of the coax. The $S12$ and $S21$ magnitude is unaffected because the change in coax insertion loss is accounted for with the cold through calibration.

V. Experimental Results

When the noise contribution of the stainless steel coaxial cable on the input and output is removed from the measured data, the resulting amplifier noise generally shows a fourfold reduction between room temperature and LN2 operation over the 4 to 8 GHz range that was measured. This is in keeping with the expected scaling of MESFET amplifier noise with ambient temperature in Kelvin—in this case 77/300. As the data in Fig. 4 show, room-temperature amplifier noise ranges from 1000 to 1350 K from 4 to 6.5 GHz. The corresponding performance while operating in the LN2 bath ranges from 250 to 350 K. Above 6.5 GHz the improvement is less consistent with the predicted temperature scaling, but still shows a significant reduction: from 1250 to 1650 K down to 350 to 550 K.

The amplifier gain increased by several dB upon cooling, as shown by the S-parameter plots of Fig. 5. As described in Section IV, there is an uncertainty in the phase reference plane of the LN2 data. However, it is believed that this error is not more than 0.1%, as only about 3/4 in. of the 8 in. coaxial lines is submerged in LN2. The $S11$ and $S22$ data indicate a general expanding of the locus on the Smith chart upon cooling, but the center of these loci remains close to 50 Ω. It is believed that this effect is caused both by the uncalibrated reduction in loss of the cold portion of the stainless steel coax and by the increase in metallization conductivity of the MMIC inductors and on-chip traces when at the LN2 temperature. This latter effect, coupled with changes in the MESFET's, contributes to the observed increase in gain and reduction in noise temperature for LN2 operation.

VI. Conclusion

We have shown that GaAs MMIC devices can be packaged to operate at cryogenic temperatures and that operation at these temperatures can lead to enhanced noise performance. In particular, the generally observed scaling of noise temperature with ambient temperature (in Kelvin) for discrete GaAs MESFET amplifiers appears to also hold for GaAs MMIC amplifiers.

Modeling of GaAs MMIC cryogenic performance should be possible if noise parameter measurements of the MESFET are made at the temperature of interest. In the case of LN2 operation, this could be accomplished on a microwave wafer probe station if fitted with an appropriate cryogen container or cold plate. The resultant modeling capability should be useful in designing MMIC circuits to interface with high-temperature superconducting devices.

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An Improved Version of the Almost Periodic Fourier Transform Algorithm with Applications in the Large-Signal Domain

J. Dreifuss, A. Madjar, and A. Bar-Lev

Abstract—**The almost periodic Fourier transform (APFT) algorithm is a useful tool in the analysis and design of nonlinear microwave circuits to which several large signals are applied simultaneously. It suffers, however, from a large spread in the calculated results. By combining the waveform balance (WB) approach with a modified form of the APFT algorithm, in which the number of randomly selected sampling points is increased, the overall computation accuracy is enhanced, the spread among results is reduced, and the computation time is practically unchanged. This modified approach is applied to the evaluation of large-signal S parameters of a MESFET and to the calculation of its 1 dB compression power, the intermodulation distortion (IMD) products, and the IP_3 points for a range of frequencies. The results are in excellent agreement with those parameters that are available from the manufacturer's measurements. The conversion gain of a MESFET mixer is also calculated and the reduced spread among the results is compared with that obtained by use of the original APFT algorithm.**

I. Introduction

The harmonic balance (HB) method has become a basic tool in modern analysis of such large-signal circuits as microwave networks employing nonlinear devices, for example power GaAs MESFET's [1], [2]. Recently, the HB method has also been used for the analysis of injection laser modulation problems [3]. The HB method overcomes the severe drawbacks of time-domain analysis, such as long transient periods that precede the steady state of interest, distributed-type circuit components which are difficult to model in the time domain, and circuits in which vastly different frequencies exist concurrently, for example, mixers. For all these cases the HB method today forms the best approach.

In the standard HB method [4] the network is divided into linear and nonlinear parts and the computation proceeds as

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The authors are with the Department of Electrical Engineering, Technion—Israel Institute of Technology, Haifa 32000, Israel.
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